

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Presented) A method of providing data
2 processor emulation information, comprising:
3 providing a program counter trace stream of program counter
4 values used by a data processor;
5 inserting a synchronization marker into the program counter
6 trace stream; and
7 providing trace information indicative of each data processing
8 operation performed by the data processor, including identifying a
9 program counter value that corresponds to the data processing
10 operation, said identifying step including expressing said
11 corresponding program counter value as an offset which indicates a
12 number of program counter values in the program counter trace
13 stream by which said corresponding program counter value is offset
14 from said synchronization marker in said program counter trace
15 stream.

Claims 2 and 3. (Canceled)

1 4. (Previously Presented) The method of Claim 1, wherein:
2 said identifying step includes detecting occurrences of
3 program counter loads in the data processor; and
4 said identifying step includes counting detected occurrences
5 of program counter loads.

1 5. (Original) The method of Claim 4, wherein said
2 identifying step includes maintaining a running count of a number
3 of program counter loads that have occurred since insertion of the
4 synchronization marker.

Claims 6 to 12. (Canceled)

1 13. (Previously Presented) An apparatus for providing data
2 processor emulation information, comprising:

3 first and second inputs for coupling to a data processor;
4 a trace stream generator coupled to said first input for
5 providing a program counter trace stream of program counter values
6 used by the data processor, said trace stream generator operable
7 for inserting a synchronization marker into the program counter
8 trace stream; and

9 a trace apparatus coupled to said second input for providing
10 trace information indicative of each data processing operation
11 performed by the data processor, including a program counter
12 identifier for identifying a program counter value that corresponds
13 to said data processing operation, said program counter identifier
14 operable for expressing said corresponding program counter value as
15 an offset which indicates a number of program counter values in the
16 program counter trace stream by which said corresponding program
17 counter value is offset from said synchronization marker in said
18 program counter trace stream.

Claim 14. (Canceled)

1 15. (Previously Presented) The apparatus of Claim 13,
2 wherein:

3 said program counter identifier is responsive to information
4 received from the data processor for detecting occurrences of
5 program counter loads in the data processor; and

6 said program counter identifier includes a counter for
7 counting detected occurrences of program counter loads.

1 16. (Original) The apparatus of Claim 15, wherein said
2 counter is operable for maintaining a running count of a number of
3 program counter loads that have occurred since insertion of the
4 synchronization marker.

Claims 17 to 22. (Canceled)

1 23. (Original) An integrated circuit, comprising:
2 a data processor for performing a data processing operation;
3 and
4 an apparatus coupled to said data processor for providing
5 emulation information about said data processing operation,
6 including a trace stream generator for providing a program counter
7 trace stream of program counter values used by said data processor,
8 said trace stream generator operable for inserting a
9 synchronization marker into the program counter trace stream, and a
10 trace apparatus for providing trace information indicative of said
11 data processing operation, said trace apparatus including a program
12 counter identifier for identifying a program counter value that
13 corresponds to said data processing operation, said program counter
14 identifier operable for expressing said corresponding program
15 counter value as an offset which indicates a number of program
16 counter values in the program counter trace stream by which said
17 corresponding program counter value is offset from said
18 synchronization marker in said program counter trace stream.

1 24. (Original) A data processing system, comprising:
2 an integrated circuit, including a data processor for
3 performing a data processing operation;
4 an emulation controller coupled to said integrated circuit for
5 controlling emulation operations of said data processor; and

6 said integrated circuit including an apparatus coupled between
7 said data processor and said emulation controller for providing
8 emulation information about said data processing operation, said
9 apparatus including a trace stream generator for providing a
10 program counter trace stream of program counter values used by said
11 data processor, said trace stream generator operable for inserting
12 a synchronization marker into the program counter trace stream, and
13 said apparatus further including a trace apparatus for providing
14 trace information indicative of said data processing operation,
15 said trace apparatus including a program counter identifier for
16 identifying a program counter value that corresponds to said data
17 processing operation, said program counter identifier operable for
18 expressing said corresponding program counter value as an offset
19 which indicates a number of program counter values in the program
20 counter trace stream by which said corresponding program counter
21 value is offset from said synchronization marker in said program
22 counter trace stream.

Claims 25 and 26. (Canceled)

1 27. (Previously Presented) The integrated circuit of Claim
2 23, wherein:

3 said program counter identifier is responsive to information
4 received from the data processor for detecting occurrences of
5 program counter loads in the data processor; and

6 said program counter identifier includes a counter for
7 counting detected occurrences of program counter loads.

1 28. (Previously Presented) The integrated circuit of Claim
2 27, wherein:

3 said counter is operable for maintaining a running count of a
4 number of program counter loads that have occurred since insertion
5 of the synchronization marker.

1 29. (Previously Presented) The data processing system of
2 Claim 24, wherein:

3 said program counter identifier is responsive to information
4 received from the data processor for detecting occurrences of
5 program counter loads in the data processor; and

6 said program counter identifier includes a counter for
7 counting detected occurrences of program counter loads.

1 30. (Previously Presented) The data processing system of
2 Claim 29, wherein:

3 said counter is operable for maintaining a running count of a
4 number of program counter loads that have occurred since insertion
5 of the synchronization marker.